

Date of Birth: 29-Oct-1985 Citizenship: Polish / Israeli
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Experience

Mobileye | Analog Design Characterization Specialist | 2023–2026 2023 – 2026

- Led post-silicon bring-up and PVT characterization of ADC/DAC blocks (~3 years) (ENOB, SNR, SNDR, THD, INL/DNL, noise, settling).
- Identified silicon corner sensitivities and performance anomalies influencing next design iterations.
- Built automated analysis/reporting pipelines and enabled remote lab operation for high-volume data evaluation.

Intel Corporation | Electrical Engineer | 2021–2023 2021 – 2023

- Developed and deployed Python-based automated test suites for high-speed interfaces (PCIe, USB4, Thunderbolt), addressing the absence of market solutions and enabling rapid industrial-grade analysis with remote lab operation. (2 years)
- Conducted PVT characterization of analog blocks (ENOB, SNR, THD, noise, BER, Eye Height/Width, Jitter), ensuring compliance and identifying performance corner cases.
- Built data pipelines and analysis tools (<http://smeas.onrender.com/>) to streamline signal processing, statistical evaluation, and reporting for complex silicon validation.

Experience continued: Qualcomm | Electrical Engineer | Audio & Analog Validation 2019 – 2021

- Led post-silicon audio and analog block validation (ADC/DAC, Pop/Click, SNR, THD, frequency response), ensuring reliable, scalable performance across PVT corners. (2 years)
- Developed calibration flows for multiple analog trims (BandGap, ADC gain/offset, voltage regulators, SMPS pulses, temperature sensors), identifying hidden bugs and enabling optimized production results.
- Collaborated with firmware, analog, and production testing engineers to correlate bench measurements with tester datalogs, resolving complex, enigmatic performance issues.

Mediatek LTD | Electrical Engineer | RF Silicon Evaluation (Contract) 2018 – 2019

- Executed post-silicon RFIC characterization and optimization, measuring key metrics (IIP2, IIP3, IRR, noise figure, gain, current consumption) across PVT conditions. (7 months)
- Automated measurement sweeps and scripted data analysis routines in MATLAB, enabling faster evaluation and reproducible results.
- Collaborated closely with RFIC designers to analyze anomalies and optimize design specifications, improving yield and performance insight.

Undisclosed company | Electrical Engineer | High-Speed I/O & Analog Systems 2017 – 2018

- Conducted post-silicon characterization and validation of high-speed interfaces (Ethernet, SERDES) and analog blocks (ADCs), ensuring precise operation across PVT corners. (13 months)
- Designed and implemented test patterns, automation scripts, and lab workflows, contributing directly to ASIC bring-up and validation efficiency.
- Extracted and analyzed measurement data to identify performance anomalies, supporting rapid design iterations and enabling reliable chip deployment.

Tel-Aviv University, and Shenkar College of Engineering, teaching assistant of electrical engineering 2016 – 2017

- Assisted in analog and electronics laboratory courses, supporting students in circuit design, signal analysis, and lab instrumentation.

Education B.Sc. at Tel-Aviv University 2010 – 2015

- Focus: Signal Processing, Analog Circuits, Communication Systems, Electro-Optics
- Final grade: 80.4/100

Studies toward B.Sc. at The Open University 2008 – 2009

- President's Honors List, 95/100

Languages English – Professional
Hebrew – Native
Thai - Conversational
Korean – Poor

Skills Post-Silicon Validation & Characterization (ADC/DAC, SERDES, RFIC)

- PVT Analysis, ENOB, INL/DNL, SNR, THD, Noise, Settling
- Lab Automation & Remote Lab Enablement (Python, MATLAB, LabVIEW, Test Scripts)
- Signal Processing & Statistical Analysis (Visualization pipelines, anomaly detection)
- Tool Development for Industrial & Research Applications (Spectral analysis, INL/DNL evaluation, Data visualization)
- High-Speed Interface Testing & Certification (PCIe, USB4, Thunderbolt)